Semiconductor Nanowires and Nanotube: Synthesis to Devices

Joshua Goldberger
Department of Chemistry, University of California, Berkeley

Semiconductor nanowire and nanotube materials are ideal, single-crystalline semiconductors that represent a facile route toward sub-100 nm features that cannot be easily fabricated through lithographic means. The usefulness of these materials lies not just in the direct miniaturization of micron-scale devices; rather, novel functionalities can be introduced by understanding and exploiting the unique electronic and optical properties intrinsic to these high surface area morphologies. Furthermore, before these materials can be utilized by the semiconductor industry, reliable, cost-effective routes for their integration into ultra-high density functional devices must be developed. My dissertation describes numerous advances in the field of nanowire and nanotube research including the rational synthesis of these materials, their incorporation into proof-of-concept electronic, photonic, and nanofluidic devices, and introduces a novel approach to enable their large-scale integration into vertically oriented, high-performance field-effect transistor (FET) devices.

'Epitaxial casting' of Inorganic Nanotubes

Previously, nanotubular materials could only be made from materials which have a layered bulk crystal structure, such as graphite, BN, MoS_2, or $NiCl_2$.[1-3] Nanotubes from these materials have inner diameters less than a few nm, often consist of multiple concentric layers, and have electrical and optical properties that depend on their growth direction. Furthermore, their synthesis typically produces mixtures of nanotubes with different growth directions and numbers of layers, which has led to enormous difficulties in characterizing their physical properties and prevented their technological application.

An 'epitaxial casting' technique is developed to enable the synthesis of single-crystalline nanotubes of materials having a traditional ionic lattice crystal structure in the bulk.[4] This synthetic approach uses nanowires as templates for the creation of core-sheath heterostuctures, followed by the selective etching of the inner nanowire core. As a first example, GaN nanotubes are synthesized through the metal-organic chemical vapor deposition of GaN thin films around ZnO nanowires grown via the vapor-liquid-solid (VLS) mechanism.[5] The ZnO nanowires are subsequently etched under reducing atmospheres (**Figure 1**). Though GaN has a wurtzite bulk crystal structure, the resultant nanotubes are single-crystalline due to the epitaxial registration

between the ZnO and GaN materials. These nanotubes have inner diameters and lengths that are the same size as the ZnO nanowires, and have shell thicknesses that can be controlled by the GaN deposition time, with minimum shell thicknesses down to 4 nm. These nanotubes are mechanically robust, have a uniform inner diameter, are electronically active, and have a high-optical quality, with little to no defect emission in the photoluminescence spectrum. Their photoluminescence characteristics are comparable to previously reported high-quality low defect GaN thin films and indicate that these nanotubes represent an ideal stress-free semiconductor system.

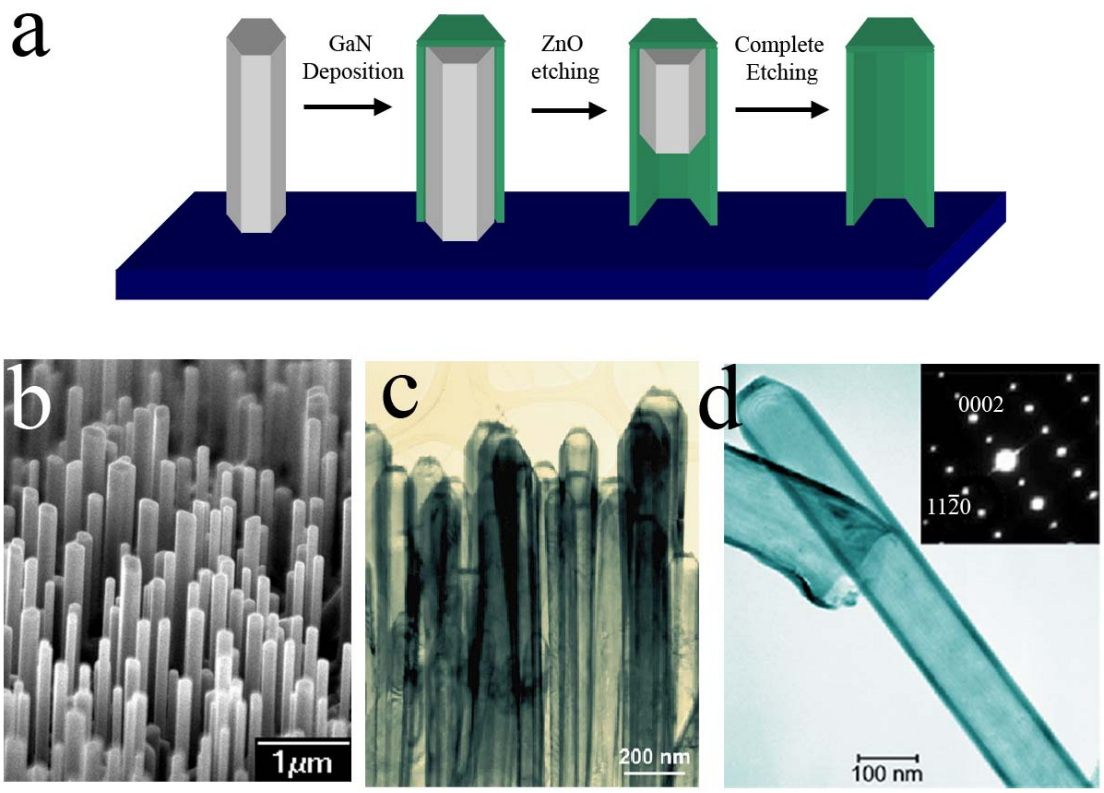

Figure 1. Synthesis of GaN nanotubes *(a)* Schematic illustration of 'epitaxial casting' process for the synthesis of GaN nanotubes. In this illustration grey corresponds to ZnO nanowire, Green corresponds to GaN nanotube, and blue corresponds to a substrate (Al_2O_3). *(b)* Scanning Electron Microscope (SEM) image of a ZnO nanowire array. *(c)* TEM image of a resulting GaN nanotube array. *(d)* TEM image of an individual GaN nanotube. Inset is the indexed electron diffraction pattern for that nanotube taken from the [-1100] zone axis, proving its single-crystalline nature. False color is added to *(c)* and *(d)* for clarity.

This 'epitaxial casting' approach is a general method for the creation of nanotubular materials for materials with any bulk crystal structure and has since been extended to numerous other materials systems.[6] Furthermore, these nanotubes represent a novel platform for the experimental study of nanofluidic transport and gating of ions in solution and biomolecular sensing in a

previously inaccessible size regime (3-100 nm), through the fabrication of microfluidic devices that are bridged by a single nanotube (**Figure 2**).[6, 7] Overall, this new class of one-dimensional nanostructures is posed to have a great impact in not only the traditional sectors of nanoscience research including photonics and electronics, but also will open up a new research paradigm in the area of nanofluidics at the bio-nano interface.

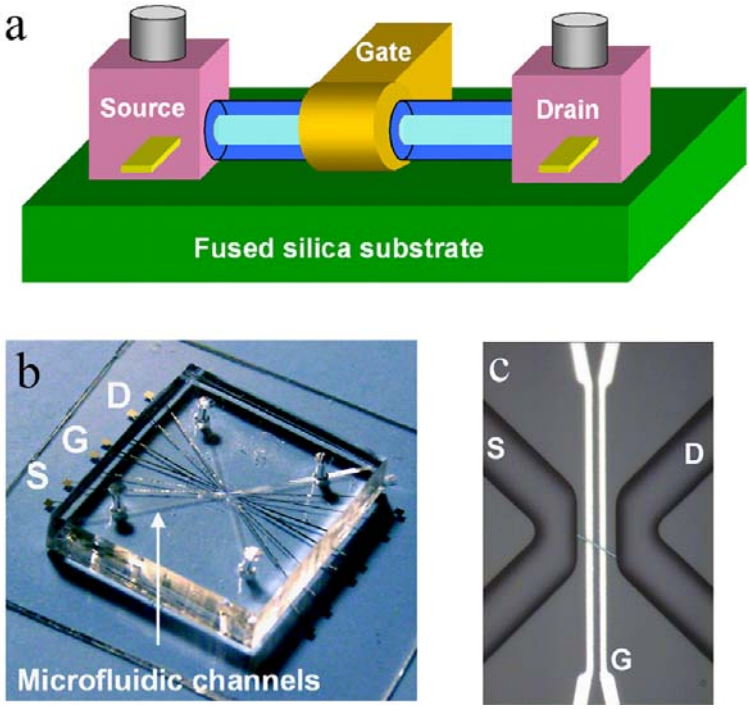

Figure 2. Single nanotube based metal-oxide-solution field effect transistors (MOSolFETs). *(a)* Schematic structure of MOSolFETs. *(b)* A fully packaged nanotube nanofluidic transistor. *(c)* A light microscopy image shows the device structure; source (S) and drain (D) microfluidic channels, the metallic gate (G), and a single silica nanotube bridging the source and drain reservoir.

Planar Nanowire Field Effect Transistors

Incorporating semiconductor nanowires as the active component in a planar horizontal FET structure both allows the detailed characterization of the nanowire electrical properties and demonstrates one potential application. As a first example, ZnO nanowires have been incorporated as the active semiconductor channels in a planar, three-terminal FET geometry with a typical back gate geometry (**Figure 3**).[8] The surface dependent device properties of ZnO nanowire transistors have been characterized. In air, these *n*-type nanowire transistors have among the highest mobilities yet reported for ZnO FETs (μ_e = 13 ± 5 cm^2 V^{-1} s^{-1}), with carrier concentrations averaging 5.2 ± 2.5 x 10^{17} cm^{-3} and on-off current ratios ranging from 10^5 to 10^7. The performance characteristics of the nanowire transistors are intimately tied to the presence and nature of adsorbed surface species (such as O_2, H_2O, and other surface species), and the FET

device performance has been evaluated in a wide variety of atmospheres, following surface cleaning procedures (including annealing, and photodesorption). Furthermore, a dynamic gate effect involving the presence of mobile surface charges causing hysteresis and time-dependent gate dissipation is characterized. These effects have been alleviated when these FET device measurements are performed in a clean, dry atmosphere following photodesorption surface cleaning.

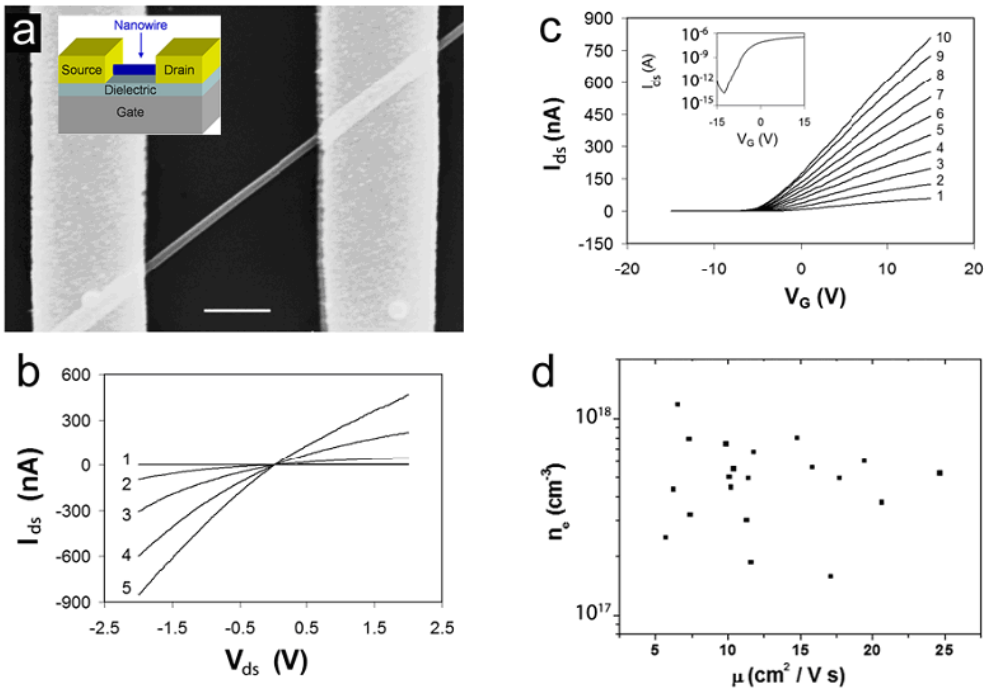

Figure 3. *(a)* SEM micrograph of a fabricated 101 nm ZnO nanowire device (scale bar = 1 μm). Inset is a schematic illustration of a bottom-gated FET device structure. *(b)* Current (I_{ds}) vs. bias voltage (V_{ds}) curves recorded at different gate voltages (V_G) for the device shown in *(a)*. Curves 1–5 correspond to a gate voltage of -10 V to 10 V, in 5 V increments, respectively. *(c)* I_{ds} vs. V_G of the same device measured at bias voltages from 0.1 to 1.0 V_{ds}. Curves 1–10 correspond to a bias voltage of 0.1–1.0 V, respectively. The inset plots I_{ds} vs. V_G measured at a bias voltage of 0.5 V_{ds} on a logarithmic scale. *(d)* Carrier concentration (n_e) vs. mobility (μ) for all transistor devices fabricated.

The electrical characteristics of numerous semiconductor nanowire materials including Si, GaN,[9] and PbX[10] (X = S, Se Te) have been evaluated in this standard FET geometry. In all of these systems, the global back-gate geometry limits the device performance and is manifested in the poor subthreshold behavior and other short channel effects, thereby leading to increased power consumption per transistor. Also, the presence of charge–trapping states and other mobile charges at or near the nanowire surface and gate dielectric result in threshold voltage shifts and degrade device performance.[11] These limitations can be overcome via the incorporation of these nanowires into surround gate FET devices, as will be discussed in the final section.

Nanowire Photonics

The electrical detection and generation of photons in structures smaller than the wavelength of light is central to the miniaturization of nanoscale integrated photonic systems for computing, communications and sensing. Chemically synthesized nanowires have several features that make them good photonic building blocks, including inherent one-dimensionality, a diversity of optical and electrical properties, good size control, low surface roughness, and, in principle, the ability to operate above and below the diffraction limit.[5] The ability to assemble photonic circuits from a collection of nanowire elements that assume different functions, such as light creation, routing, and detection is an essential goal for nanowire photonics. Therefore, ZnO nanowire photodetectors and GaN nanowire LEDs are fabricated for their incorporation into an "all-nanowire" photonic circuit.

Initial studies of ZnO nanowire photodetectors utilized devices where the nanowire electrical properties are characterized by having large contact resistance Au-ZnO schottky barrier contacts.[12] UV excitation of the nanowires increased their carrier concentration via direct electron hole pair creation and the photodesorption of electron-trapping species from the nanowire surface.[13] The ZnO nanowires used in our FET devices behave similarly, and a five order of magnitude change in resistance is observed upon direct excitation with a UV laser (**Figure 4**). As an initial proof-of concept, these ZnO photodetectors are able to electrically detect the emission of light that is transmitted through SnO_2 nanoribbon waveguide routers.[14]

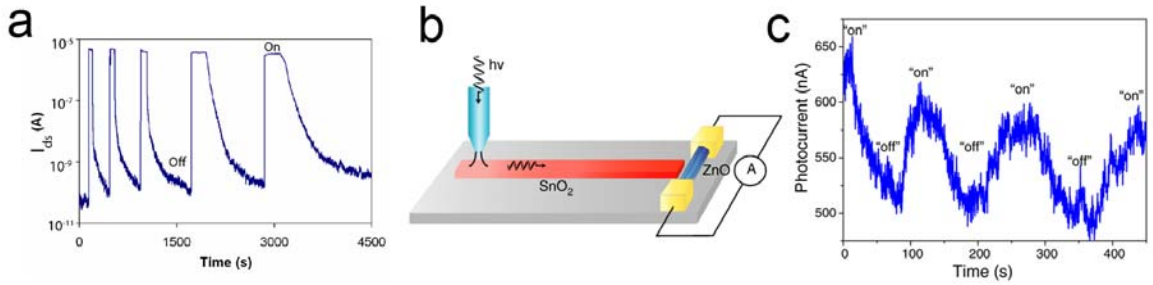

Figure 4. Photodetection properties of ZnO FET and integrated electrical detection of light. (a) Reversible switching of a ZnO nanowire between low and high conductivity states when a He:Cd laser operated at 325 nm was used as the UV light source. The bias on the nanowire is 1 V. (*b*) Schematic drawing of the integration of a nanoribbon waveguide with a photodetector. Light launched into a ribbon waveguide with a near-field probe is detected via the photocurrent response of an adjacent ZnO nanowire photodetector. (*c*) Detector response as the near-field tip was scanned repeatedly on and off of the nanoribbon while exciting it at 325 nm. Variations in signal amplitude were due to slow detector response and slight differences in the location of the tip on the nanoribbon surface.

Finally, nanowire-based LEDs using n-type GaN nanowires are fabricated by assembling n-type semiconductor nanowires onto pre-fabricated p-type Si lines that were etched from silicon-on-insulator (SOI) substrates (**Figure 5**). Room temperature electroluminescence emission from

the n-type GaN nanowire is observed to emit directly from the p-Si/n-GaN pn-junction. In the future, practical photonic devices will require the integration of nanoribbon waveguides with a variety of high-efficiency electrically-driven nanowire light sources and photo detectors with different band gaps. Nevertheless, these experiments are the first to demonstrate the feasibility of integrating nanowire based photoemission, optical routing and, photodetection on the same platform.

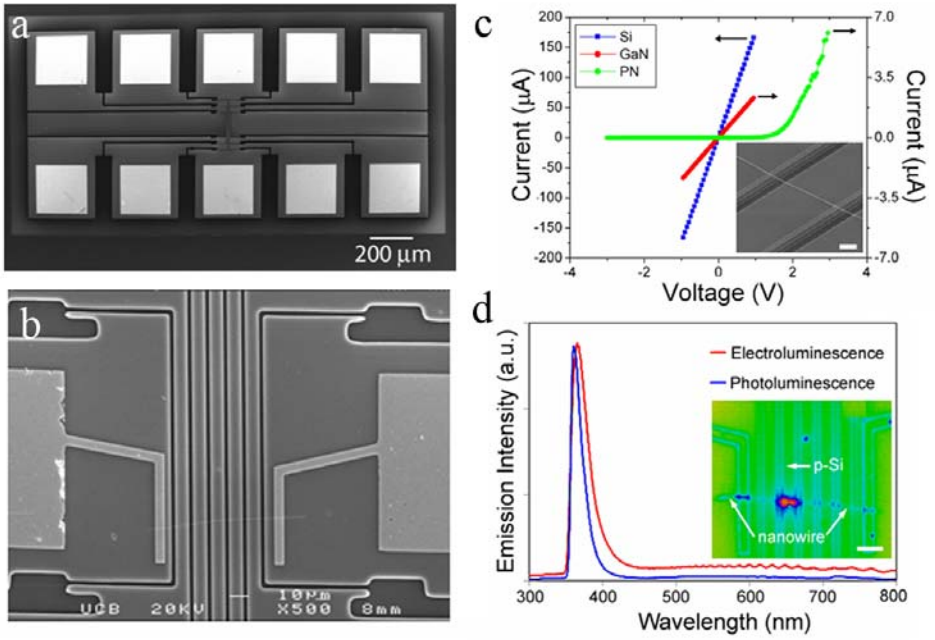

Figure 5. Nanowire LED on SOI pattern. (a) SEM image of p-type silicon trench structure consisting of five electronically isolated Silicon lines. (b) close up SEM image of a finished device (c) The room temperature IV curve through the p-Si line (blue curve), n-GaN nanowire (red curve) and the p-Si/n-GaN pn-junction (green curve). Inset is an SEM image of the nanowire-silicon interface (scale bar = 2 µm). (d) The photoluminescence spectrum and the electroluminescence spectrum taken from the GaN wire on the device. Inset is the light emission pattern from the 2nd LED (scale bar = 10 µm).

Vertically Integrated Nanowire Field Effect Transistors (VINFET)

The amount of energy and time required to align and integrate nanowire components into high-density planar FET circuits still remains as the most significant hurdle preventing widespread application. To overcome this problem, the bottom-up in-place growth of nanowires is combined with top down very-large-scale-integration (VLSI) processing, thereby eliminating the need for any subsequent post-growth assembly techniques.

The controlled, epitaxial synthesis of vertically aligned silicon nanowire arrays from silicon (111) substrates has been achieved (**Figure 6**).[15] The nanowires were synthesized in a home-built chemical vapor deposition system, which uses $SiCl_4$ as the precursor gas, BBr_3 as a dopant source, and gold colloids as VLS catalysts. These nanowire arrays have average diameters down

to 39 nm, with narrow diameter distributions dictated by the distribution of the seeding colloids thereby indicating that each nanowire is grown by only one nanoparticle. The growth position of these nanowire materials can be controlled via accurate placement of these nanoparticle catalysts.

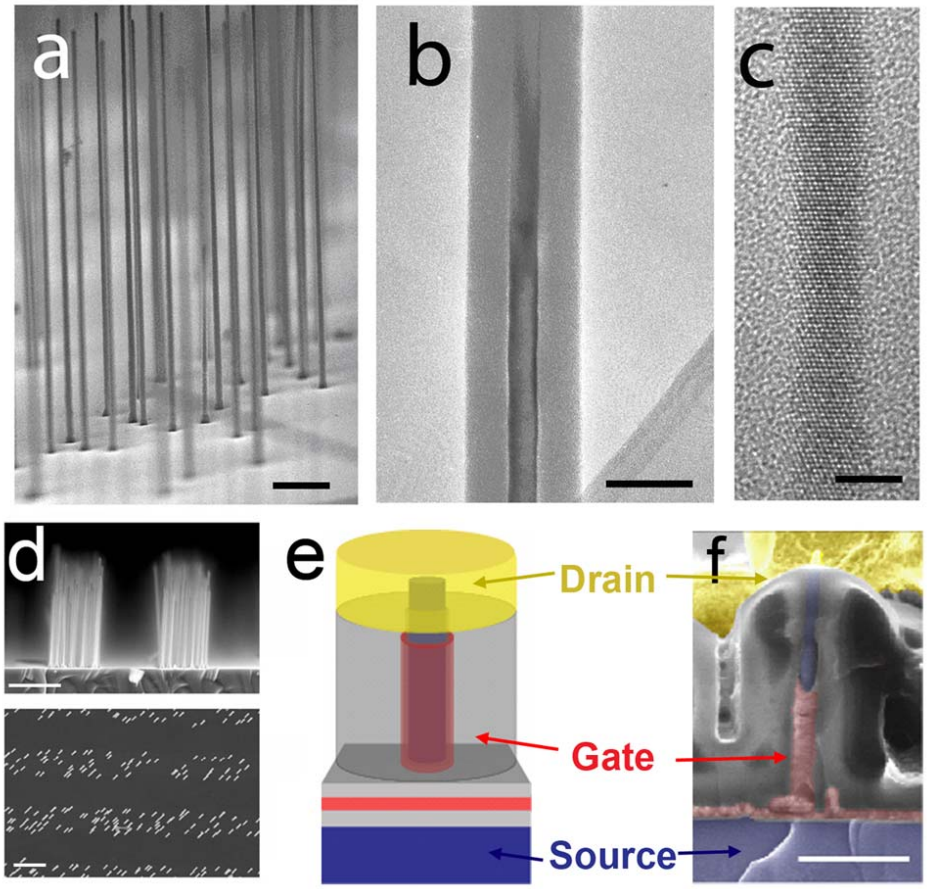

Figure 6. VINFET Device Configuration. *(a)* Cross-sectional SEM image of vertically grown Si nanowires off of a Si (111) substrate. Scale bar is 1 μm. *(b)* TEM image of Si nanowire surrounded in a conformal SiO_2 coating after dry oxidation at 850 ^oC to form the gate dielectric. Scale bar is 75 nm. *(c)* High-resolution TEM image of a Si nanowire with an inner diameter that has been reduced to ~4.5 nm. Scale bar is 4 nm. *(d)* Cross-sectional (above) and top-down SEM image (below) showing patterned Silicon nanowire growth dictated via soft-lithographic patterning of the Au catalyst (Scale bars are 2 μm). *(e)* Schematic illustration of VINFET device structure. *(f)* Cross-sectional SEM image of a VINFET device (Scale bar is 500 nm). False color is added to image *(f)*, for clarity. In *(e)* and *(f)*, blue corresponds to the Si source and nanowire, grey corresponds to SiO_2 dielectric, red corresponds to the gate metal, and yellow corresponds to the drain metal.

These nanowires are then directly integrated into surrounding-gate FETs using conventional VLSI processing.[16] The device fabrication allows Si nanowire channel diameters to be readily reduced to the 5-nm regime. These first-generation VINFETs exhibit electronic properties that are already comparable to planar MOSFETs and may, with further optimization and engineering, compete with advanced solid-state nanoelectronic devices (**Figure 7**).

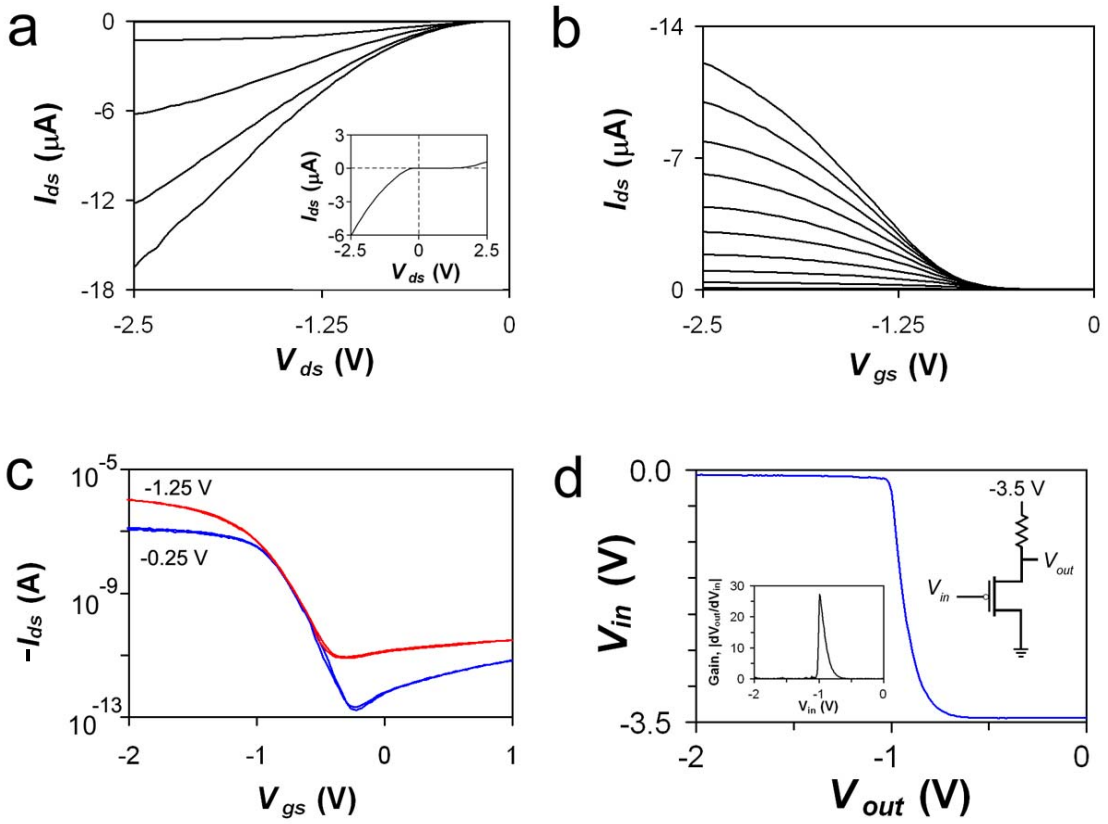

Figure 7. VINFET Device Characteristics. *(a)* I_{ds} vs. V_{ds} at V_{gs} = -2.5 V to -0.5 V in 0.5 V steps from bottom to top. Inset shows the full I_{ds} vs. V_{ds} spectrum at V_{gs} = -1.5 V. *(b)* I_{ds} vs. V_{gs} with V_{ds} ranging from -2.5 V to -0.25 V in 0.25 V steps, from top to bottom, respectively. The curves collected in *(a)* and *(b)* are from a device having 131 nanowires connected in parallel. *(c)* I_{ds} vs. V_{gs} at -1.25 V_{ds} (red) and -0.25 V_{ds} (blue), for a device having 20 nanowires collected in parallel, and measured by varying V_{gs} from negative to positive to negative values at a 10 mV/s rate. This device has minimal hysteresis, a subthreshold slope of ~120 mV/decade and an I_{on}/I_{off} ratio > 10^5. *(d)* Output characteristics of an inverter circuit (right) fabricated with a p-type VINFET device with 20 nanowires connected in parallel and an external 200 MΩ resistor. An inverter gain of ~28 is determined from the first derivative of this plot with respect to V_{in} (left).

Conclusion

This dissertation describes numerous fundamental advances in the field of nanowire and nanotube research ranging from synthesis to their incorporation into electronics, photonics, and nanofluidics. This work has opened up new directions in basic research, and has demonstrated novel approaches to exploit the unique properties of one-dimensional materials and easily integrate them into high-performance devices.

1. Iijima, S., *Nature* **1991,** 354, (6348), 56-58.

2. Patzke, G. R., Krumeich, F., Nesper, R., *Angew. Chem., Int. Ed. Engl.* **2002,** 41, (14), 2446-2461.

3. Tenne, R., Zettl, A. K., Nanotubes from inorganic materials. In *Carbon Nanotubes*, 2001; Vol. 80, pp 81-112.

4. Goldberger, J., He, R. R., Zhang, Y. F., Lee, S. W., Yan, H. Q., Choi, H. J., Yang, P. D., *Nature* **2003,** 422, (6932), 599-602.

5. Law, M., Goldberger, J., Yang, P. D., *Annu. Rev. Mater. Res.* **2004,** 34, 83-122.

6. Goldberger, J., Fan, R., Yang, P. D., *Acc. Chem. Res.* **2006,** 39, (4), 239-248.

7. Fan, R., Karnik, R., Yue, M., Li, D. Y., Majumdar, A., Yang, P. D., *Nano Lett.* **2005,** 5, (9), 1633-1637.

8. Goldberger, J., Sirbuly, D. J., Law, M., Yang, P., *J. Phys. Chem. B* **2005,** 109, (1), 9-14.

9. Kuykendall, T., Pauzauskie, P., Lee, S. K., Zhang, Y. F., Goldberger, J., Yang, P. D., *Nano Lett.* **2003,** 3, (8), 1063-1066.

10. Fardy, M., Hochbaum, A. I., Goldberger, J., Zhang, M., Yang, P., **Submitted**.

11. Vashaee, D., Shakouri, A., Goldberger, J., Kuykendall, T., Pauzauskie, P., Yang, P. D., *J. Appl. Phys.* **2006,** 99, (5), 054310.

12. Kind, H., Yan, H. Q., Messer, B., Law, M., Yang, P. D., *Adv. Mater.* **2002,** 14, (2), 158-+.

13. Collins, R. J., Thomas, D. G., *Phys. Rev.* **1958,** 112, (2), 388-395.

14. Law, M., Sirbuly, D. J., Johnson, J. C., Goldberger, J., Saykally, R. J., Yang, P. D., *Science* **2004,** 305, (5688), 1269-1273.

15. Hochbaum, A. I., Fan, R., He, R. R., Yang, P. D., *Nano Lett.* **2005,** 5, (3), 457-460.

16. Goldberger, J., Hochbaum, A. I., Fan, R., Yang, P. D., *Nano Lett.* **2006,** 6, (5), 973-977.